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(54) Low-noise bipolar transistor.

(57) A low-noise transistor comprising a cutoff region (38; 47) laterally surrounding the emitter region (36; 45) in the surface portion of the transistor and of such conductivity as to practically turn off the surface portion of the transistor, so that the transistor operates mainly in the bulk portion. In the NPN transistor, the cutoff region is formed by a P ring (38) in a P^- type well region (35), and, in the PNP transistor, by the N^+ type enriched base region (47) between the emitter region (45) and the collector region (49).

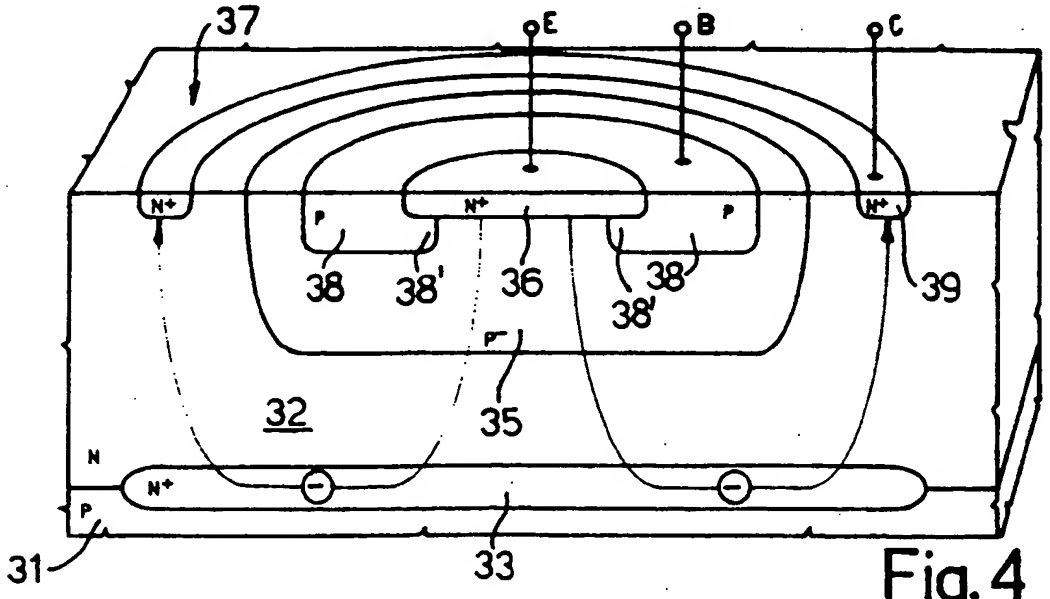

Fig. 4

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The present invention relates to a low-noise bipolar transistor.

As known, in electronic devices, the term "noise" indicates a random fluctuation in currents or voltages at the device terminals, and may seriously limit the minimum signal level that can be handled by the device.

The noise in each device is due to various physical causes, some of which have been known for some time. Of particular interest are what are known as "flicker" noise (also indicated 1/f) and "burst" noise, the first of which exists in all and the second in a significant percentage of devices.

Flicker noise is commonly acknowledged to be caused by fluctuations in the number of carriers, due to entrapment of the carriers in surface layers of the device, i.e. to tunneling at the semiconductor-oxide interface. According to accepted theory, the carriers in the semiconductor may communicate with trap levels at a given distance within the tunnel oxide layer, and remain trapped for some time prior to being re-emitted. In the case of transistors, in particular, flicker noise sources are located at the base-emitter junction.

Flicker noise is especially undesirable in the case of operational amplifier input transistors and audio preamplifiers.

Burst noise, on the other hand, is caused by a sharp variation in current between two or more constant values. Variation frequency may be very low (less than 1 Hz) or high (hundreds of herz), in which case, burst noise may be confused with a high degree of flicker noise. This type of noise is generally attributed to the presence of defects, metal inclusions and precipitates in the space charge region of the junction; and the fluctuation in current depends on the extent, if any, to which the defect participates in conduction. The fact that burst noise is reduced by deficiency-reducing processes, such as gettering, would appear to bear out this theory.

In the case of flicker noise, the noise power at the output terminals of a transistor is proportional to I_B^{α}, where I_B is the base current and α a constant ranging between 1 and 2. In the case of burst noise, the output noise power is inversely proportional to the square of the gain of the transistor, so that, for a given collector current, high-gain transistors are less affected by flicker and burst noise as compared with low-gain types.

One proposal already made for reducing flicker and burst noise is to produce extremely high-gain (super-beta SBT) transistors with a gain typically ranging between 1000 and 10,000 for collector currents below 1 μA. In NPN type super-beta transistors, the base layer is narrower as compared with standard transistors, for improving the base transfer factor (reducing recombination of the charge carriers) and so increasing gain. In a planar process, in particular, by reducing the base width (thickness of the P type base layer between the N^+ type emitter region and the N type epitaxial layer) to roughly 0.2-0.3 μm (as compared with the normal 0.8 μm), current gain increases to as much as 2000-5000 (as compared with 200-300).

High-gain NPN transistors may be produced simultaneously with conventional NPN types by adding a photolithography and diffusion step to the planar process. In practice, following base diffusion of the conventional NPN transistor, windows are opened photolithographically, and through the windows the emitter of the high-β_F transistors is predeposited and partially diffused. This is followed by photolithography and diffusion of the conventional emitter, so that the emitter of the high-β_F transistors is deeper than that of the conventional ones, thus considerably reducing the thickness of the active base (by way of comparison, refer to Figures 1 and 2 relative to a standard and a high-gain transistor, in which w_B and w_B' indicate the respective base widths).

High-gain transistors of the aforementioned type, however, present an extremely low (roughly 3 V) open-base collector-emitter breakdown voltage (BV_{CEO}),and cannot be employed in applications requiring a higher voltage, due to the risk of punch-through between the emitter and collector.

Moreover, prediffusion increases the likelihood of emitter pipes being formed, due to penetration of an emitter portion inside the base region as far as the collector, as a result of crystallographic defects. As known, such pipes so modify the I_C-V_{CE} output characteristics of the transistor that they become resistive. This problem is particularly felt in the case of power integrated circuits, even to the extent of eliminating the advantages of high gain, or resulting in production rejects and, hence, reduced efficiency.

A further drawback lies in the need for providing an additional masking step as compared with the standard fabrication process, thus increasing fabrication costs.

Another known noise reducing solution consists in producing transistors with a high A_E/P_E ratio, i.e. a high ratio of the area and perimeter of the emitter region visible from above, so as to reduce the contribution of the surface portions with respect to that of the deep regions (bulk). This solution, however, only provides for reducing flicker and is ineffective as regards burst noise.

It is an object of the present invention to provide a transistor designed to overcome the drawbacks posed by known solutions, and which, in particular, provides for reducing the noise on transistors by means of a flexible solution, adaptable to various requirements, and ensuring high

breakdown voltages.

According to the present invention, there is provided a low-noise bipolar transistor as claimed in Claim 1.

In practice, the transistor according to the present invention operates solely in the bulk portion and very little in the surface portion, thus minimizing flicker noise with no reduction in breakdown voltage and, at least in most cases, with no need for additional masks.

Moreover, in the case of NPN transistors, the base portion in which the transistor operates is less heavily doped as compared with known transistors, thus reducing recombination and, hence, increasing gain, and so also reducing burst noise.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a cross section in perspective of a silicon wafer featuring a known type of NPN transistor;

Figure 2 shows a cross section in perspective of a silicon wafer featuring a high-gain NPN transistor;

Figure 3 shows a cross section in perspective of a silicon wafer featuring a known type of PNP transistor;

Figure 4 shows a cross section in perspective of a silicon wafer featuring an NPN transistor in accordance with the present invention;

Figure 5 shows a cross section in perspective of a silicon wafer featuring a PNP transistor in accordance with one embodiment of the present invention;

Figure 6 shows a cross section of a silicon wafer featuring a PNP transistor in accordance with a further embodiment of the present invention.

Figure 1 shows a standard NPN transistor with a P type substrate 1; an N type epitaxial layer 2; an N^+ type buried layer 3; an N^+ type enriched collector region 4; a P type base region 5; and an N^+ type emitter region 6. w_B indicates the width of base region 5.

Figure 2 shows a known high-gain NPN transistor of the same structure as in Figure 1, with a substrate 11; an epitaxial layer 12; a buried layer 13; an enriched collector region 14; a base region 15; and an emitter region 16. As can be seen, emitter region 16 is deeper than the corresponding region 6 in Figure 1, so that base width w_B' of base region 15 is less than the corresponding base width w_B in Figure 1.

Figure 3 shows a known PNP transistor with a P type substrate 21; an N type epitaxial layer 22; a junction isolation region 23 (formed by a bottom portion 23a and a top portion 23b on account of the two-step fabrication process); a buried layer 24; a P type emitter region 25; a P type collector region 26; a P^-type ring 27 surrounding collector region 26 (P-well 27); and an N^+ type enriched region 28 at the base contact.

The known transistor in Figure 3 presents considerable surface phenomena resulting in flicker noise; and a high total base resistance (including enriched region 28, epitaxial layer 22 and buried layer 24) resulting in less than optimum noise levels.

Figure 4 shows an NPN transistor in accordance with the teachings of the present invention, and which is formed in a silicon wafer comprising a P type substrate 31; an N type epitaxial layer 32; and an N^+ type buried layer 33 interposed between substrate 31 and epitaxial layer 32 at the active area of the transistor. Inside epitaxial layer 32, there are formed a P type well region 35, less heavily doped as compared with the others and so indicated P^-; an N^+ type emitter region 36 inside well region 35 and facing surface 37 of the wafer; a P type annular region 38, also formed inside well region 35, facing surface 37 and laterally surrounding emitter region 36; and an N^+ type enriched region 39 at the collector contact.

Figure 4 also shows schematically the emitter, base and collector contacts E, B and C.

In the Figure 4 transistor, annular region 38 (which, together with well region 35, forms the base region) presents substantially the same doping level as base region 5 of standard transistors (R_s of about a hundred Ω/[]) so that the peripheral portion of the base region presents the same characteristics as the standard base region 5. Conversely, well region 35 presents a much lower doping level as compared with annular region 38 (R_s of a few KΩ/[]), and is much deeper than the standard base region 5 (typical depths from surface 37 for emitter region 36, annular region 38 and well region 35 are 1.5 μm, 1.8 μm and 3 μm respectively). As a result, the central portion of the emitter region sees a less heavily doped and deeper portion as compared with the structure of known transistors.

Well region 35 is formed prior to the base diffusion step (in this case, resulting in annular region 38) which is performed by predeposition and subsequent diffusion of boron atoms.

By virtue of annular region 38 about emitter region 36, and the less heavily doped portion 35 facing emitter region 36, operation of the peripheral surface region of the transistor is reduced, and the transistor operates mainly in the bulk portion, which is deeper as compared with the known structure (the path of the charges - in this case, electrons - is shown by the arrows). As a result, in the effectively operative base region, recombination is reduced and gain increased (to 1000-1500), thus reducing both flicker and burst noise. Flicker noise

is also limited by virtue, as already stated, of the surface portion of the transistor operating very little, so that the traps in the oxide overlying surface 37 of the wafer and in the surface layer are rendered ineffective.

For the structure to be effective, it is important that annular region 38 be contiguous not only laterally but also with a portion of the bottom surface of emitter region 36, so that a portion (indicated 38' in Figure 4) of annular region 38 overlaps emitter region 36. The overlap area may be so calculated as to minimize the efficiency of the surface transistor. In fact, current distribution between the surface transistor and the bulk transistor depends, not only on dope concentration, but also on the ratio between the area of emitter region 36 facing well region 35, and the overlap area of emitter region 36 and portion 38'.

The Figure 4 structure is highly flexible in that, by varying the concentration and depth of well region 35, and the ratio between the area of annular region 38 and the area of well region 35 at the central emitter portion, it is possible to vary breakdown voltage, gain and the noise levels as required in relation to the functions being implemented.

The Figure 4 structure may be used in any precision circuit wherein high gain is required (e.g. current mirror and band-gap circuits), but in which given breakdown voltage BV_{CEO} values must be ensured.

In general, the Figure 4 structure requires an additional mask for forming well region 35. In most power circuits, however, a P-well layer is already provided at some point, so that such a mask is already included in most fabrication processes. If such is the case, the Figure 4 structure simply involves modifying the existing mask, with no need for additional fabrication steps, and hence no increase in cost, as compared with traditional processes. Even if the rest of the circuit integrated in the same chip presents no P-well regions, however, the disadvantage of providing an additional mask is more than compensated for by the considerable improvement in performance obtainable.

Figure 5 shows a first embodiment of a PNP transistor in accordance with the present invention, wherein the transistor is formed in a silicon wafer including a P type substrate 41; an N type epitaxial layer 42; an N^+ type buried layer 43; and a P^+ type junction insulation region 44 (formed by a bottom portion 44a and a top portion 44b on account of the two-step fabrication process). Inside epitaxial layer 42 and facing surface 51 of the wafer, there are formed: a P^+ type emitter region 45; a P type annular region 46 surrounding and contiguous with emitter region 45; an N^+ type enriched base region 47 surrounding and contiguous with annular region 46; a P^- type well region 48 surrounding and contiguous with enriched base region 47; a P^+ type deep collector region 49 surrounding and contiguous with well region 48; and a P type internal collector region 50 inside deep collector region 49, but facing surface 51 of the wafer, for connection to collector contact C. Figure 5 also shows schematically the base and emitter contacts B and E.

In the Figure 5 transistor, location of the enriched base region 47 between emitter region 45 and collector region 49-50 provides for predominantly bulk operation of the transistor, i.e. in the deep inner portion of the epitaxial layer, and for cutting off the surface portion of the transistor, as shown schematically by the arrows indicating the path of the charge carriers (in this case, holes). In this case also, as with the NPN transistor in Figure 4, non-participation of the surface portion in the transfer process provides for reducing flicker noise.

Location of enriched base region 47 close to emitter region 45 also provides for considerably reducing base resistance, thus further reducing flicker noise.

In the Figure 5 transistor, P type annular region 46 between emitter region 45 and enriched base region 47 is required for avoiding an N^+/P^+ junction, which, as known, involves current leakage. Similarly, well region 48 prevents current leakage between regions 47 and 49.

Collector region 49 is formed simultaneously with top portion 44b of junction isolation region 44, so that no additional masks are required. Deep portion 49 is required for the emitter region to "see" a sufficient collector area and ensure adequate current collection. On the other hand, the emitter area must be minimum, compatible with etching requirements, for preventing high gain of the parasitic vertical PNP transistor (formed by substrate 41, buried layer 43, epitaxial layer 42 and emitter region 45). Internal collector region 50 is not essential to operation of the lateral PNP transistor, and is provided solely for ensuring the thickness of the oxide over the collector region, at the point in which the contacts are opened, is equal to that of the oxide over regions 45 and 47.

The Figure 5 structure requires no additional masks as compared with the standard process. In fact, as already stated, deep collector region 49 is formed simultaneously with top portion 44b of junction isolation region 44; internal collector region 50 is equivalent to standard transistor collector region 26 (Figure 3) and is formed simultaneously with annular region 46; and a P-well mask is already included in the standard process (for forming standard transistor region 27 - Figure 3).

Following P implantation on substrate 41 for forming bottom portion 44a of isolating region 44, and N diffusion for forming buried layer 43, a

typical process for fabricating the Figure 5 transistor therefore includes, in sequence: growing epitaxial layer 42; simultaneously forming top portion 44b of isolating region 44 and deep collector region 49; forming well region 48; forming annular region 46; and forming emitter region 45 and enriched base region 47.

In the Figure 5 transistor, channel width W_B between regions 46 and 48 is subject to a certain amount of inaccuracy, due to the distance between annular region 46 and well region 48 possibly varying as a result of misalignment of the respective masks. To solve this problem, an alternative structure may be employed as shown in Figure 6, which is identical to that of Figure 5 (and the corresponding regions of which are therefore indicated using the same numbering system), with the exception of P type annular region 46, which, in Figure 6, is replaced by a less heavily doped annular well region 46'. Annular region 46' is formed using the same mask as for well region 48, so that channel width W_B' is unaffected by misalignment of the masks.

In the Figure 6 transistor, the gain of the parasitic vertical PNP transistor is also reduced by reducing the doping level of region 46' as compared with region 46. The area of annular well region 46' must, however, be minimum, for the purpose, as before, of maintaining the gain of the parasitic transistor as low as possible.

To those skilled in the art it will be clear that changes may be made to the transistor and relative fabrication process as described and illustrated herein without, however, departing from the scope of the present invention.

Claims

1. A low-noise bipolar transistor comprising an emitter region (36; 45), a base region (35, 38; 42, 47) and a collector region (32, 39; 49, 50) integrated in a layer of semiconductor material (32; 42) defining a surface portion and a deeper bulk portion; characterized by the fact that it comprises a cutoff region (38; 47) laterally surrounding said emitter region (36; 45) in said surface portion, for operating the transistor predominantly in said bulk portion.

2. An NPN type transistor as claimed in Claim 1, characterized by the fact that it comprises:
   - a P type annular region (38) in said surface portion; said annular region surrounding and being contiguous with the lateral surface and part of the bottom surface of said emitter region (36), so as to define a portion (38') underlying said emitter region; said annular region presenting a first doping level; and
   - a P type base portion (35) surrounding and contiguous, at least at the bottom, with said emitter region (36) and said annular region (38); said base portion presenting a second doping level lower than said first doping level.

3. A transistor as claimed in Claim 2, characterized by the fact that said base portion (35) presents a resistivity of a few KΩ/[]; and said annular region (38) presents a resistivity of about a hundred Ω/[].

4. A transistor as claimed in Claim 2 or 3, characterized by the fact that said base portion (35) is formed by a well region; and said annular region (38) is formed by a base diffusion.

5. A transistor as claimed in one of the foregoing Claims from 2 to 4, characterized by the fact that said annular region (38) is deeper than said emitter region (36) and roughly half the depth of said base portion (35).

6. A PNP type transistor as claimed in Claim 1, characterized by the fact that said base region comprises an N type annular region (47) surrounding said emitter region (45) and located in said surface portion; and at least a portion of said layer of semiconductor material (42); said layer of semiconductor material being N type, and presenting a third doping level; and said annular region (47) presenting a fourth doping level higher than said third doping level.

7. A transistor as claimed in Claim 6, characterized by the fact that said N type annular region (47) is connected to a base contact (B).

8. A transistor as claimed in Claim 6 or 7, characterized by the fact that said collector region comprises a deep annular layer (49) formed by an upper isolating diffusion embedded in said layer of semiconductor material (42) and laterally surrounding said N type annular region (47).

9. A transistor as claimed in one of the foregoing Claims from 6 to 8, wherein said emitter region (45) is a P type and presents a fifth doping level; characterized by the fact that it comprises a P type annular layer (46; 46') located in said surface portion between and contiguous with said emitter region (45) and said annular region (47); said annular layer presenting a sixth doping level lower than said fifth level.

10. A transistor as claimed in one of the foregoing Claims from 6 to 9, characterized by the fact that it comprises a P type well region (48) located in said surface portion between and contiguous with said annular region (47) and said collector region (49).

11. A transistor as claimed in Claims 9 and 10, characterized by the fact that said well region (48) presents the same doping level and the same depth as said annular layer (46').

12. A process for fabricating a transistor as claimed in Claim 1, comprising an emitter region (36; 45), a base region (35, 38; 42, 47) and a collector region (32, 39; 49, 50) integrated in a layer of semiconductor material (32; 42) defining a surface portion and a deeper bulk portion; characterized by the step of forming a cutoff region (38; 47) in said surface portion of said layer of semiconductor material; said region laterally surrounding said emitter region (36; 45) and operating the transistor mainly in said bulk portion.

13. A process as claimed in Claim 12, for fabricating a transistor as claimed in one or more of the foregoing Claims from 2 to 6; characterized by the fact that it comprises the steps of:
- forming a P type well region (35) in a layer of N type semiconductor material;
- forming, in said well region and said surface portion, a P type annular region (38) of a higher doping level as compared with said well region;
- forming said N type emitter region (36) in said annular region and said surface portion.

14. A process as claimed in Claim 12, for fabricating a transistor as claimed in one or more of the foregoing Claims from 6 to 11; characterized by the fact that it comprises the steps of:
- simultaneously forming an upper isolating region (44b) and a deep annular collector region (49) in a layer of N type semiconductor material (42);
- forming, in said layer of semiconductor material (42) and said surface portion, a P type emitter region (45) surrounded at a distance by said deep collector region (49); and
- forming, in said layer of semiconductor material and said surface portion, an N type annular region (47) interposed between said emitter region and said deep collector region.

15. A process as claimed in Claim 14, characterized by the fact that it also comprises the steps of:
- forming, in said layer of semiconductor material (42) and said surface portion, a P type intermediate region (46; 46') between and contiguous with said emitter region (45) and said annular region (47); said intermediate region (46) presenting a lower doping level as compared with said emitter region; and
- forming, in said layer of semiconductor material and said surface portion, a P type well region (48) between and contiguous with said annular region (47) and said collector region (49).

16. A process as claimed in Claim 15, characterized by the fact that said steps of forming said intermediate region (46') and said well region (48) are performed simultaneously using the same mask.

17. A process as claimed in Claim 15, characterized by the fact that it comprises the step of forming an annular contact region (50) inside said deep collector region (49); said steps of forming said annular contact region (50) and said intermediate region (46) being performed simultaneously using the same mask.

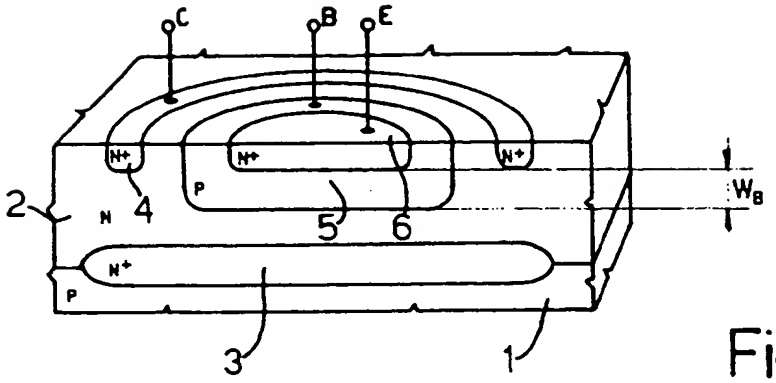

Fig.1

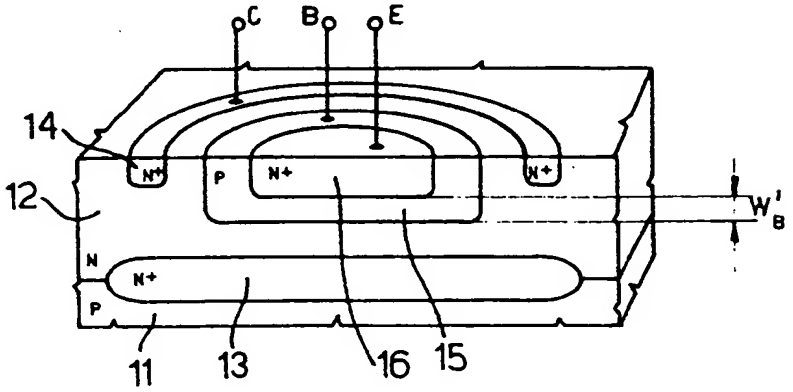

Fig.2

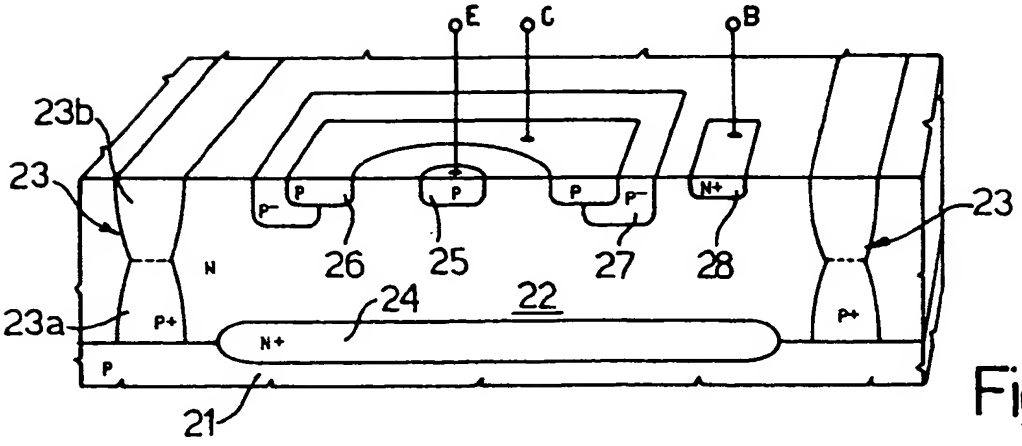

Fig.3

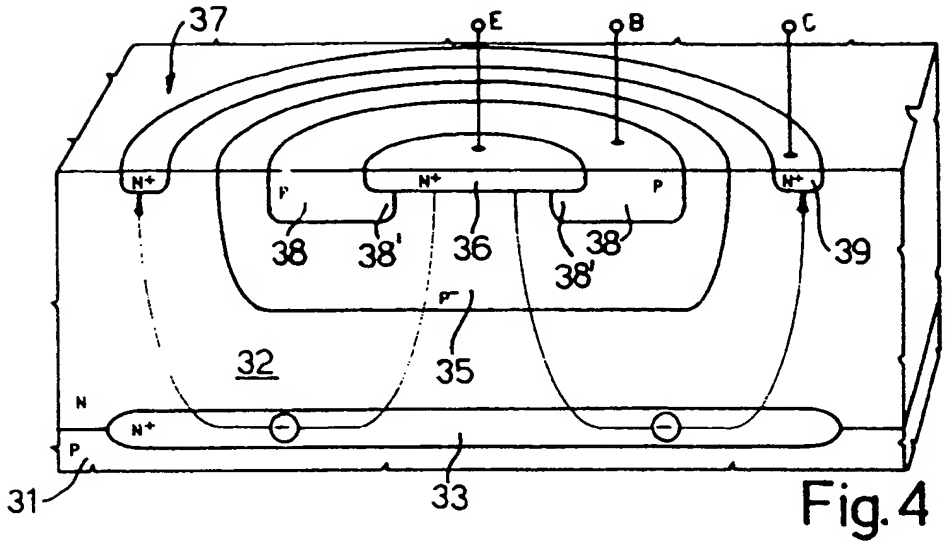

Fig.4

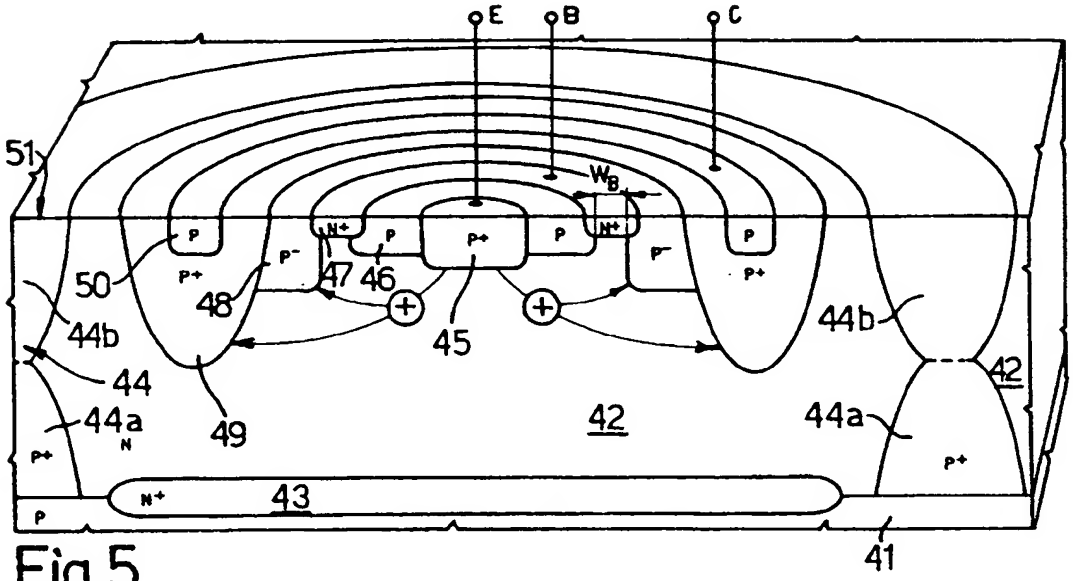

Fig.5

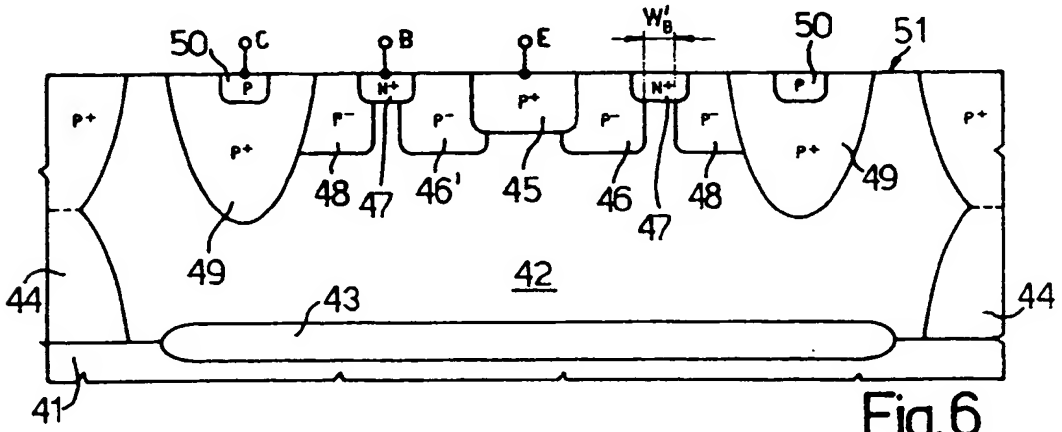

Fig.6

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EUROPEAN SEARCH REPORT

Application Number
EP 93 83 0393

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 029 548 (SIEMENS AKTIENGESELLSCHAFT) * abstract; figure 5 *	1,2,5,12	H01L29/10 H01L29/73
X	DE-A-26 34 618 (LICENTIA PATENT-VERWALTUNGS-GMBH) * page 9, line 6 - page 12, line 15; figures 1-4 *	1-4,12, 13	
X	US-A-4 047 217 (MCCAFFREY ET AL.) * column 4, line 27 - column 7, line 25; figures 2,5-9 *	1,2,4,5, 12,13	
A	EP-A-0 435 331 (SONY CORPORATION) * abstract; figure 1 *	6	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 February 1994	Baillet, B

CATEGORY OF CITED DOCUMENTS

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